Multi-Band Synthesizer, Power Amplifier, and Filter Development Final Report

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1. Introduction

This final report describes three research and development projects conducted by Synergy Microwave Corporation for DARPA (Defense Advanced Research Agency). The purpose of these projects was to develop and demonstrate the key sub-systems needed for an ultra-high performance, low cost, multi-band tactical transceivers. These devices include: 1) A 25 MHz to 2,500 MHz, 5 W power amplifier, 2) A 2.5 GHz to 6 GHz synthesizer to be used the receiver's first local oscillator, and 3) A 25 MHz to 3,000 MHz tunable filter that can be used as a pre-selector or a post power amplifier filter.

The report has five chapters. The first chapter is an introduction. The second chapter describes the amplifier. The third chapter describes the synthesizer. The fourth chapter describes the filter. The fifth chapter provides a summary.

2. Broadband Distributed Power Amplifier Development

2.1 Scope of Work

To design and develop a Broadband power Amplifier in the frequency range 25 MHz to 2500 MHz with output power of about 5 Watt (CW) using Distributed Amplifier technique.

2.2 Design Methodology

There are number of broadband techniques are available in practice. This includes the conventional broadband impedance matching techniques such as transmission line transformers. Ladder networks, stepped impedance structures, and more popular distributed traveling wave amplifiers widely used in the microwave frequency range.

The conventional networks are good up to 1 GHz, which use RF power transistors including LDMOS structures but are not suitable for frequency range extending beyond 1 GHz and also they are very bulky. Distributed Amplifiers using traveling wave structures are widely used in the microwave frequency range up to 18GHz but mainly for low output power due to device constraints. Recently it has been reported by a device manufacturer CREE Microwave packaged SiC based MESFETs capable of high break down voltage, which is highly essential for high power applications operable up to S-band. This device is capable of providing an output power of up to 10 Watts in S-band. Compared to these SiC based MESFETs the conventional GaAs based MESFETs are not capable of providing wideband operation and also high output power due to the device limitations. Based on detailed literature survey (1…4), it was concluded that SiC MESFETs are more suitable for our application and it would be preferable to use Distributed Amplifier technique compared to conventional design approaches for the limitations listed above.

2.3 Principle of Operation:

A schematic of distributed Amplifier is shown in Figure 1.

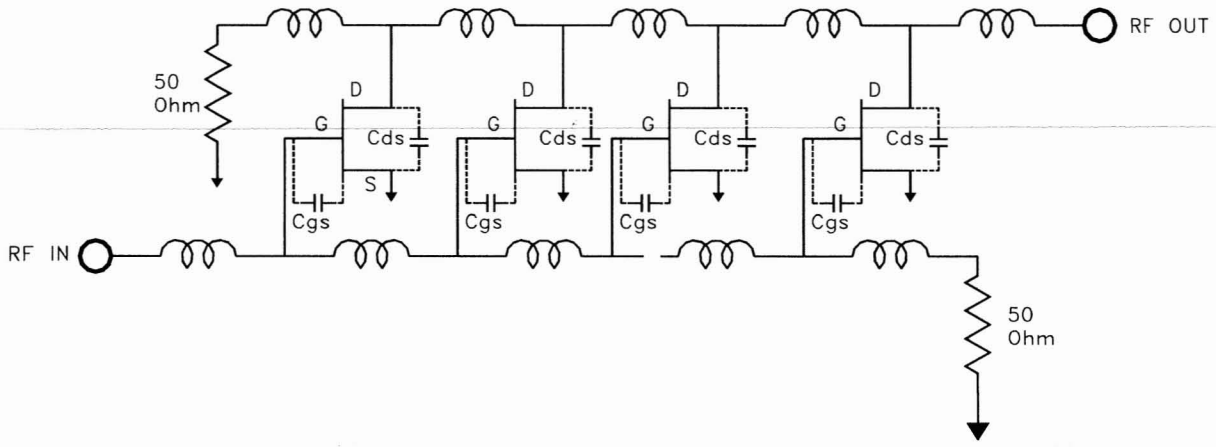


Figure 1: Schematic of Distributed Amplifier

A Distributed Amplifier, also known as Traveling Wave amplifier is designed by cascading number of discrete transistors in a suitable way to increase the Gain-Bandwidth product of the amplifier. This is achieved by combining the input and output capacitances of the transistor with inductors or equivalent transmission lines between Gates and Drains of the transistors. The gate and drain impedances are absorbed by these transmission lines (known as gate and drain lines), thereby widening the bandwidth. Input signal is fed at port1 to the gate of the first transistor and the output is taken from the drain of the last transistor. The drain of the first transistor and the gate of the last transistor are terminated in 50 ohms. An RF signal applied at the input end of the gate line travels down to the terminated end where it is absorbed. As the signal travels voltage wave and the amplified signal is coupled to the next device through the drain line. If the phase velocities on the gate and drain lines are identical, then the signals on the drain line add in the forward direction as they arrive at the output. The waves traveling in the reverse direction are not in phase and any uncancelled signal is absorbed by the drain line termination. Thus the signal fed at the input gate terminal is coherently amplified at the output drain terminal. By proper choice of the device in terms of breakdown voltage and limiting parasitic capacitances and inductances it is possible to achieve broadband amplifiers with bandwidth up to 10: 1.

2.4 SiC MESFET based Distributed Amplifier Design

The design goals are given below:

1. Frequency Range: 25 MHz to 2500 MHz
2. Gain: 12 – 14 dB
3. Output Power: 5 Watts(Typ)
4. Input/Output VSWR: 2: 1(Typ)

The device chosen for the development was from CREE with part no.CRF-2010-101(SiC RF Power MESFET. The small signal gain of the device is 12 dB and 10W minimum P1dB (power at 1 dB gain Compression). The Based on the device equivalent circuit parameters and available small signal S-Parameters, a 4-stage distributed Amplifier was designed. The design calculations show that the device capacitance between Gate and Source (Cgs) is so large that

device cannot operate in broadband mode beyond 1.2 GHz. Further, the computer aided analysis show that due to package parasitic, the device tend to oscillate around 800 MHz and this further limits the extendable frequency range on the upper end. The optimized circuit file and the estimated performance are shown in Figure 2 and Figure 3.

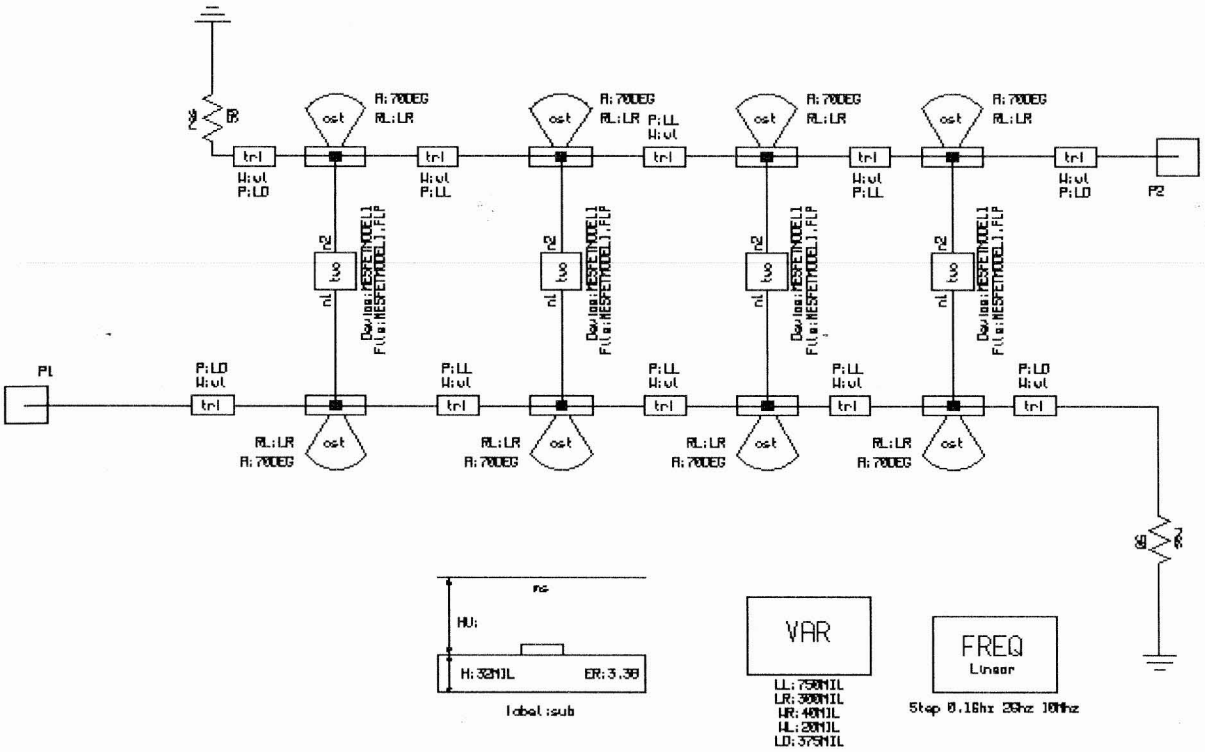


Figure 2: Schematic Diagram of SiC MESFET 4- Stage Distributed Amplifier

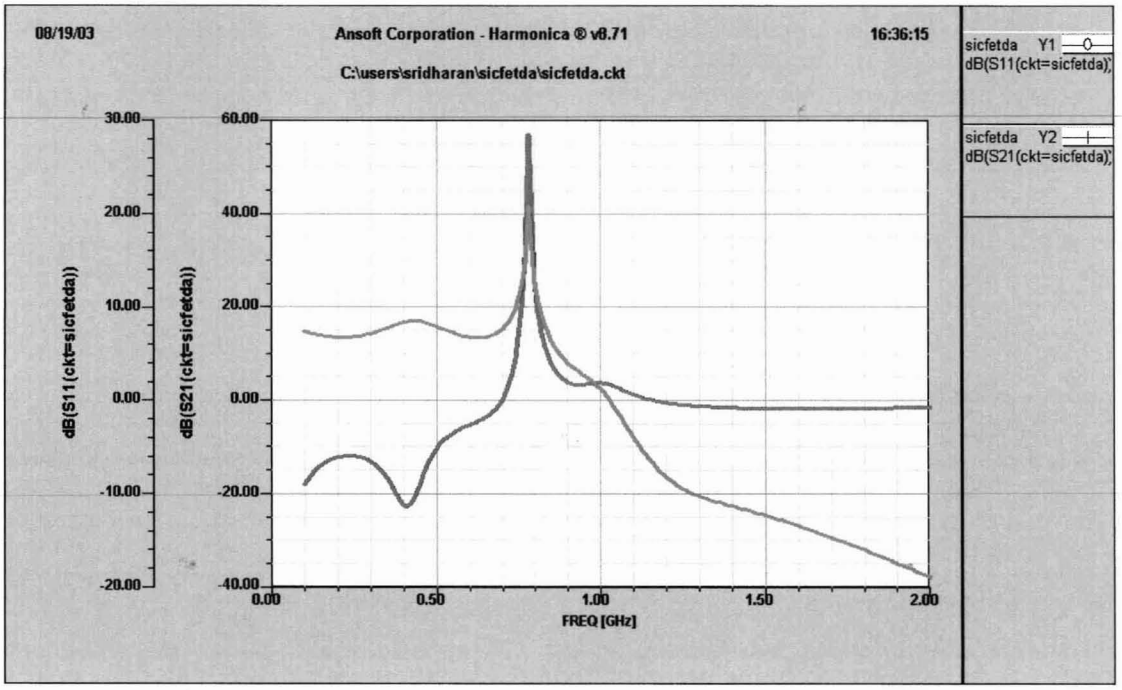


Figure 3: Gain and Return Loss Performance (Simulated)

In order to demonstrate the high power capability of SiC MESFETs over a wide range, the design was fabricated which include networks to suppress oscillations. The final fabricated unit on heat sink and the performance plots are shown in Figure 4, Figure 5, and Figure 6.

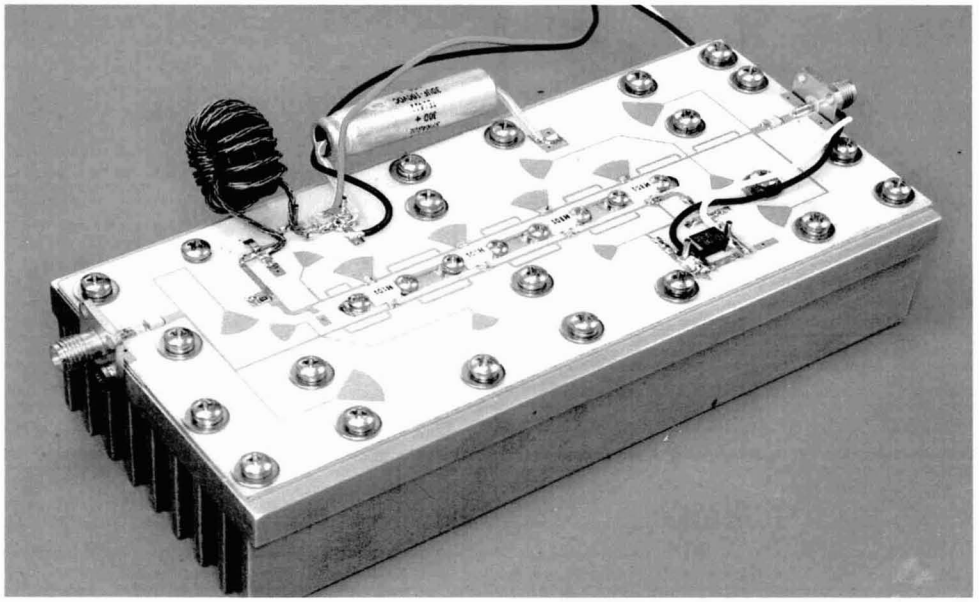


Figure 4: Assembly of SiC MESFET 4-Stage Distributed Amplifier

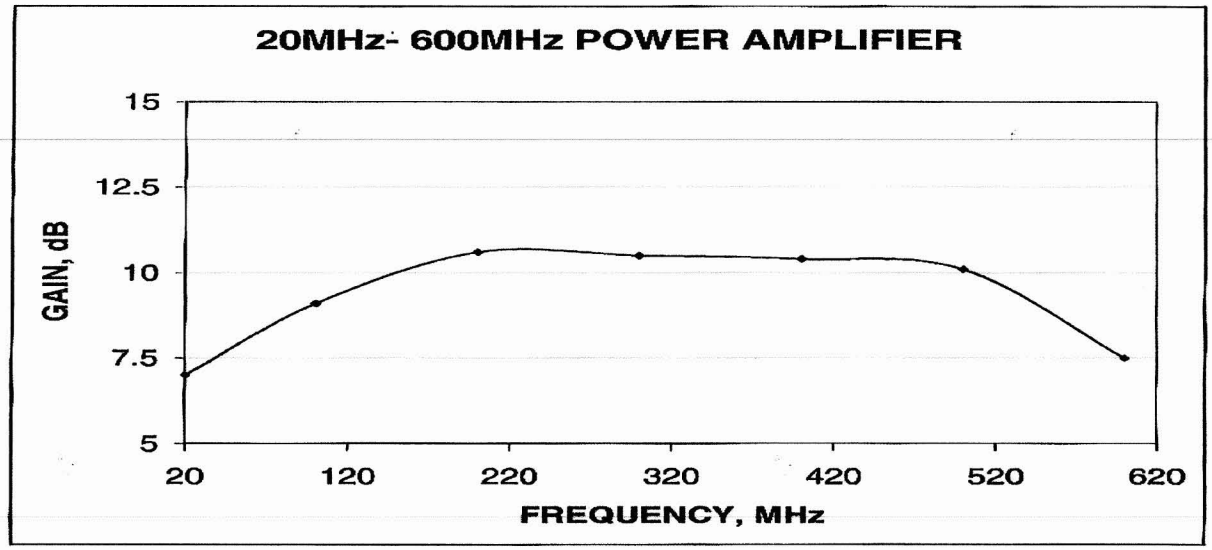


Figure 5: Gain and Return Loss Performance of 4-Stage SiC MESFET Distributed Amplifier (Measured)

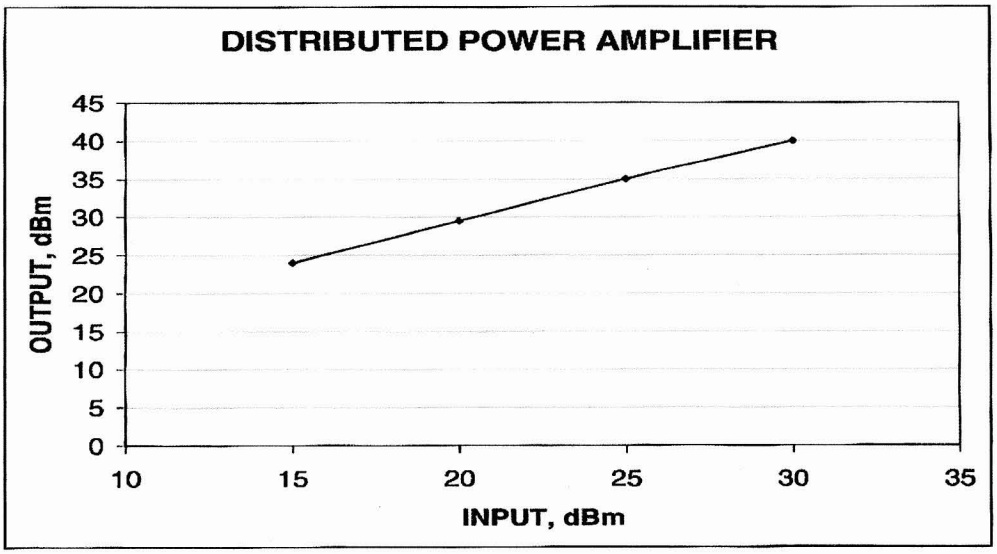


Figure 6: Output Power vs. Input Power (Measured)

The gain plots clearly indicate the limitation at high frequency end beyond 600 MHz caused by device parasitic. A detailed discussion through correspondence was conducted with CREE to understand and resolve the problem. CREE engineers fully supported our findings and expected an unpackaged device in die form would provide better performance. But they expressed their inability to provide in die form, as it is not available yet. Further, the for the packaged device, the gate lead inductance is of the order of 0.45nH and drain inductance is about 0.33nH which are undesirable for our application leading to oscillation at high frequencies. So while it was possible for us to demonstrate the high power and reasonably broadband

characteristics of SIC MESFETs when used as Distributed Amplifiers, the shortcomings at high frequency end are mainly due to device limitations.

2.5 Distributed Amplifier using GaAs MESFETs

In our study of Distributed Amplifier using SiC MESFETs, it was absorbed that gate-source capacitance (Cgs) is preferred to be low to achieve wide band performance. Since CREE was not having the device in die form, and they are still working on it, we thought it is appropriate to use GaAs MESFETS usable up to Ku band and with low value for Cgs. However, the limitation is the output power capability of these devices. The device with required capacitance characteristics can only deliver 0.25 Watt. But it was decided to study the scope of distributed amplifier approach for our application, while waiting for the correct device from CREE.

A four stage distributed amplifier using FLK027 from Fujitsu was designed and developed. The Schematic diagram is shown in Figure 7, and simulated results are shown in Figure 8. It is seen that where the device has no oscillations in the frequency range of interest, thereby meeting the wide bandwidth requirements, it is limited only by the output power capability. The fabricated unit is shown in Figure 9, and the measured performance is shown in Figure 10, Figure 11, and Figure 12.

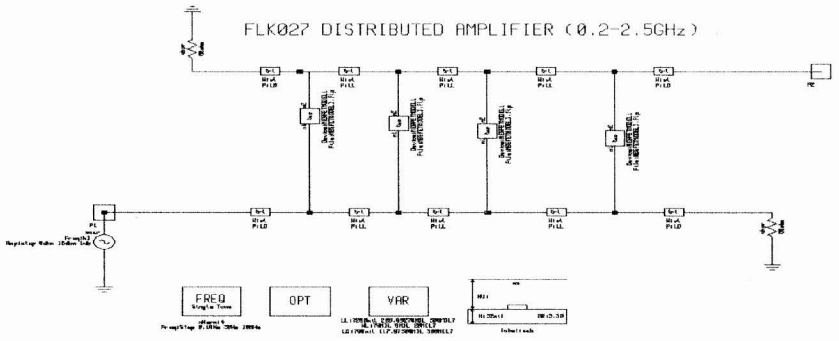


Figure 7: Schematic of GaAs MESFET Distributed Amplifier

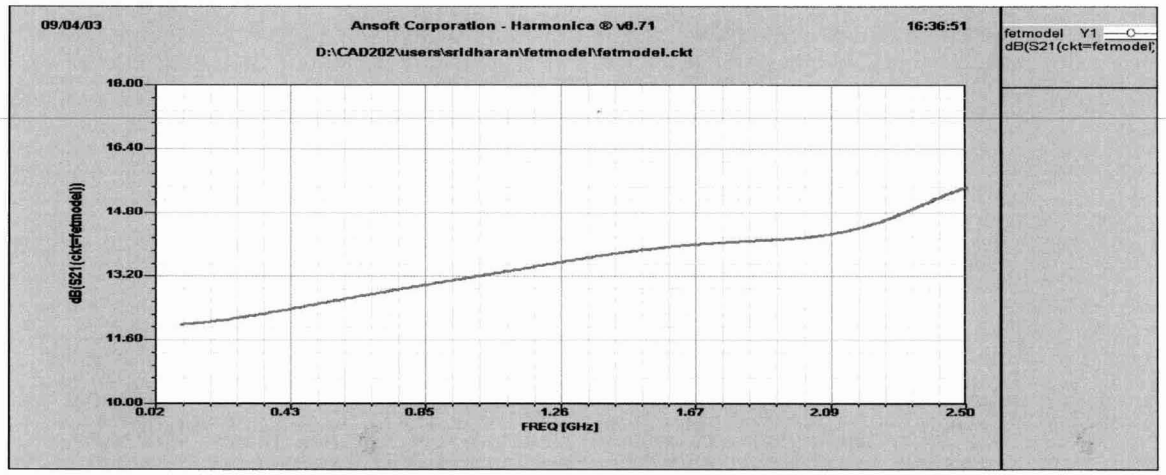


Figure 8: Gain vs. Frequency (Simulated)

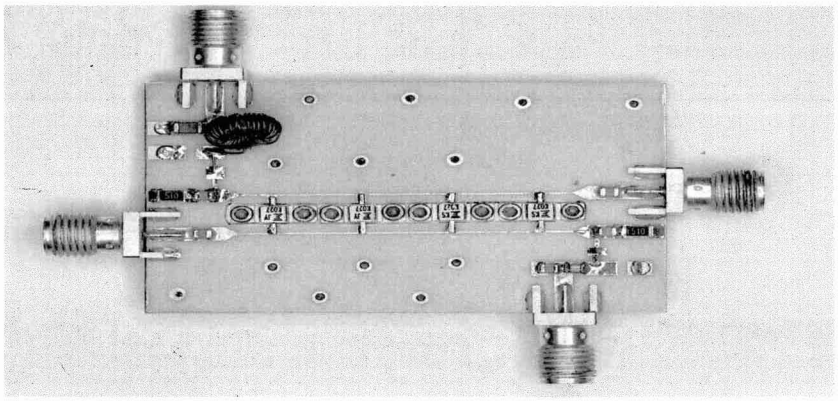


Figure 9: GaAS MESFET Distributed Amplifier Assembly

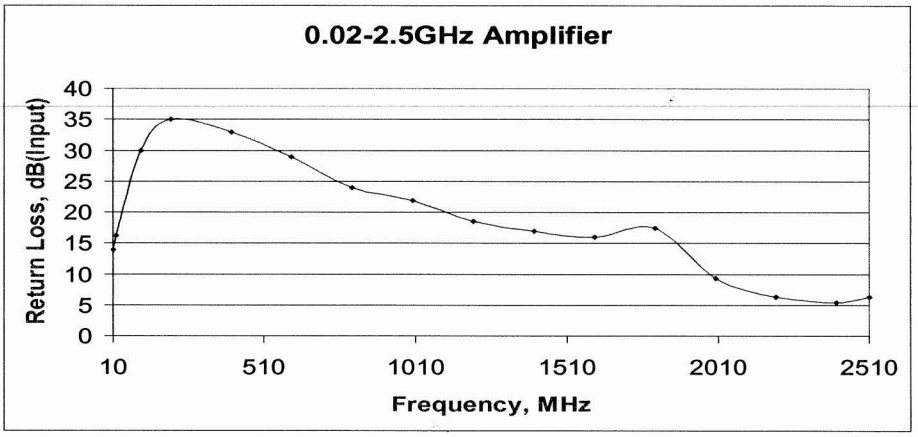


Figure 10: Return Loss Performance of GaAS MESFET Distributed Amplifier (Measured)

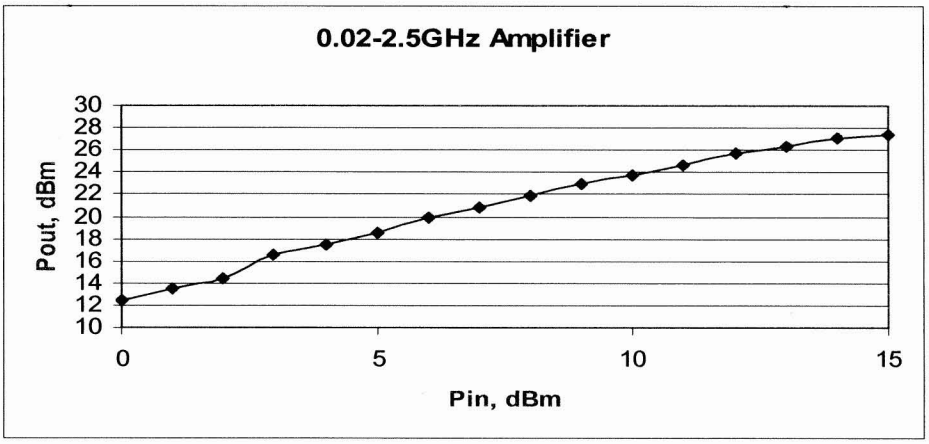


Figure 11: Power Output Performance of GaAS MESFET Distributed Amplifier (Measured)

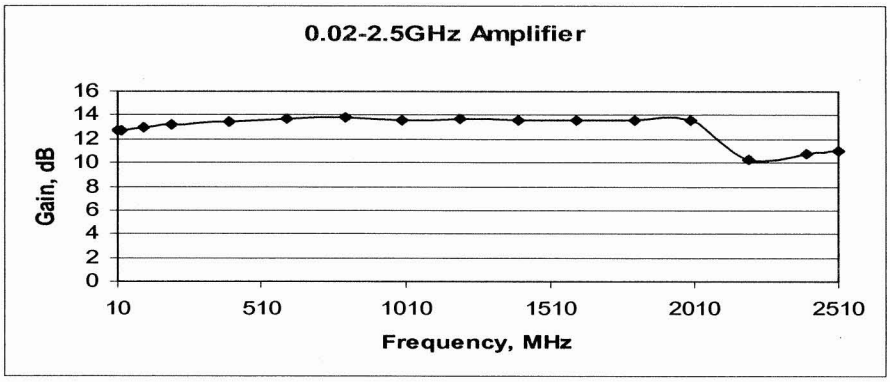


Figure 12: Gain Performance of GaAS MESFET Distributed Amplifier

2.6 Conclusion

High Power capability of Distributed Amplifiers over a restricted bandwidth was demonstrated through the first design using packaged SiC MESFETs from CREE. The wide bandwidth capability of the design approach was further demonstrated through the second design using available GaAs MESFETs. The study carried out clearly demonstrates the limitations to meet the design goals are mainly due to non-availability of devices with low Cgs, high breakdown voltage and more importantly in die form to eliminate package parasitic. Based on our continuous interaction with device manufactures including CREE we understand the work is still progress and no device to meet our requirement are available at present.

3. Broadband, Low Phase Noise Synthesizer Development

3.1 Scope of work

Design target was the design of a low phase noise 2.5-6 GHz synthesizer with lowest possible phase noise and current consumption.

3.2 Design

The challenge of this type of synthesizer is to achieve excellent performance in a small size with moderate current consumption using commercially available components.

Several approaches were studied and the most promising designs were realized and measured.

A key component of a synthesizer is the VCO. It has to provide the desired wideband tuning range as well as low phase noise.

Under this contract under inclusion of own funding the following wideband VCO's were designed:

- 350-1050 MHz, 0.9x0.9" size, -112 dBc phase noise @ 10 kHz
- 600-1800 MHz, 0.5"x0.5" size, -105 dBc phase noise @ 10 kHz
- 1.5-3.2 GHz, 0.5"x0.5" size, -95 dBc phase noise @ 10 kHz
- 1.9-4.1 GHz, 0.5"x0.5" size, -90 dBc phase noise @ 10 kHz

A 3GHz to 6GHz VCO, 0.5"x0.5" is still under design funded from own resources and will be made available to the public during 2005.

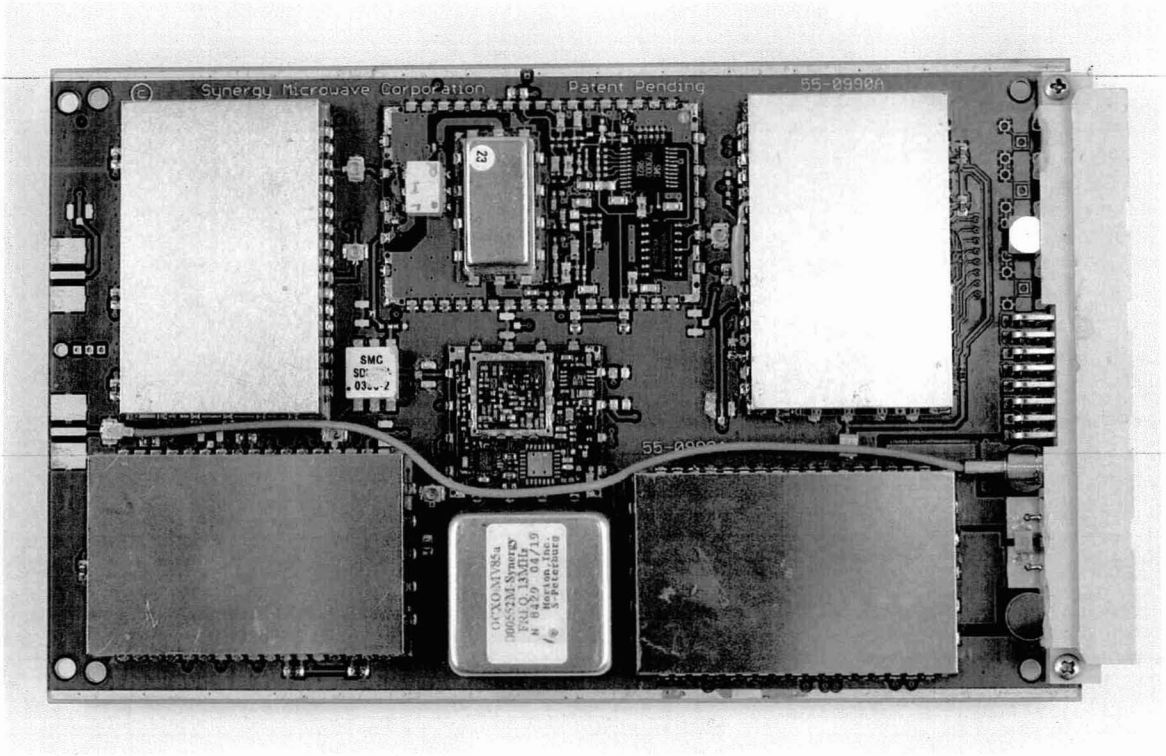
Another promising way to achieve low phase noise at high frequencies is the use of a Push-Push VCO. Here two VCO's running at half the desired frequency are coupled in a way that the resulting output frequency is the sum of both VCO frequencies. As both VCO's are on exactly the same frequency and their noise is non-coherent the resulting noise on the output frequency is lower then the phase noise of the individual oscillator. The main problem in such a design is to keep the phase difference between the two VC) sections exactly 90deg to achieve the best possible performance. To achieve this a special phase detector and steering circuit was developed. Due to the unavailability of commercial IC's for the desired frequency range the functionality was only shown at lower frequencies. If IC's are made available or designed from own resources this type of oscillator will be completed.

As the phase noise of the VCO itself isn't sufficient in close proximity of the carrier (up to ~150kHz) the PLL has to provide a much lower phase noise to be able to reduce the resulting noise floor up to frequencies of 150kHz.

Due to the 1Hz step size requirement a DDS chip has to be used. The DDS can only provide frequencies up to ~100MHz with a noise floor of ~-120dBc and a spurious suppression of –90dBc at best. As this, directly translated to the desired frequency range, would not satisfy the requirements a different solution had to be developed.

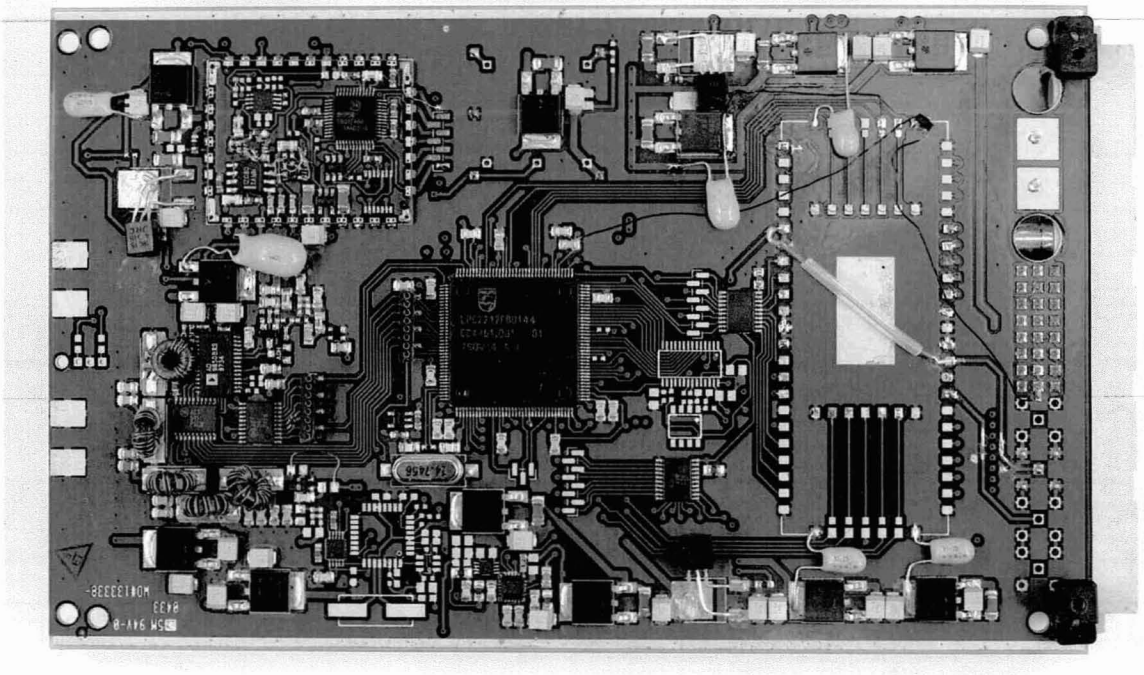
Even without the 1 Hz resolution requirement the translation of the phase noise to frequencies up to 6 GHz would not allow achieving the required phase noise.

Top View of Final Prototype



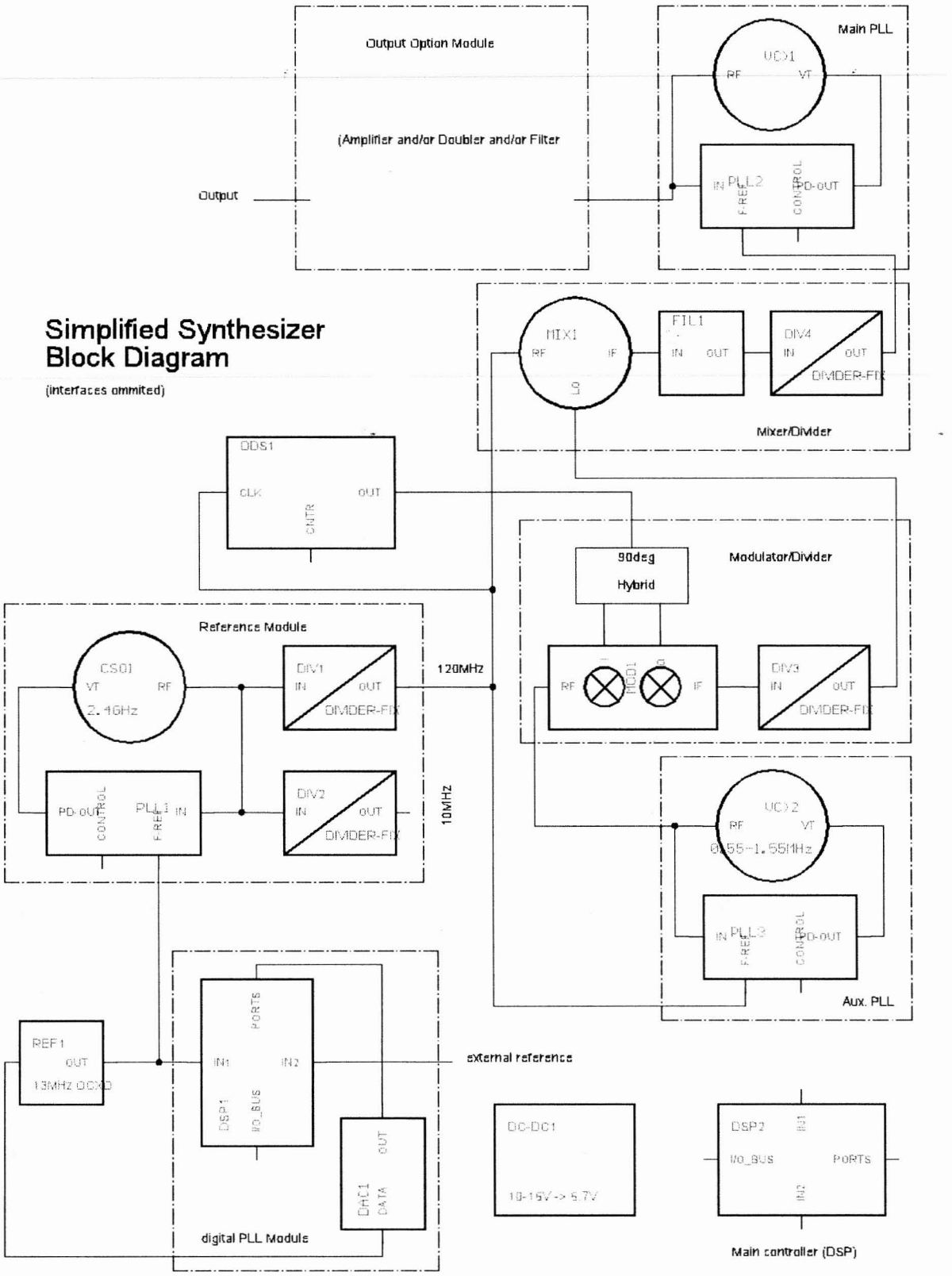
Top, left to right: Modulator/Divider, Mixer/Divider, Main Synthesizer
Center: Auxiliary Synthesizer
Bottom: Reference Module, OCXO, Switchmode Power Supply
(some modules w/o cover to show internal complexity).

Bottom View of Final Prototype



Center: Digital Signal Processor
Left: DDS
Right: output module (not implemented) like an amplifier or doubler

Block Diagram of Final Prototype



The core of the system is a ceramic resonator based oscillator (fixed frequency) that provides a noise floor of –130dBc and better at 2.4GHz. This clean frequency is used to drive all other functions of the synthesizer. To achieve the desired frequency stability it is phase locked to an oven controlled crystal oscillator (OCXO), which again can be locked to external frequency references.

The output signal of the DDS is mixed in a modulator (to suppress the carrier and one sideband) with the Auxiliary Synthesizer to a frequency of ~550MHz to 1.55GHz, then divided down to ~5MHz-8MHz. This frequency is then mixed with the clean 2.4GHz/20=120MHz and divided again by 5 resulting in a frequency range around 25MHz variable in steps of less then 1Hz. By mixing and dividing noise and spurious get suppressed and the resulting frequency is used as a variable, very clean reference for the Main Synthesizer. It converts the reference up to the desired frequency range, depending on which VCO is used.

The synthesizer in the picture above uses the 1.9 to 4.1GHz VCO and provides a phase noise of ~-95 dBc@10kHz from the carrier at 4.1GHz. The phase noise is limited by the Main Synthesizer PLL chip and can be improved by at least 15dB if a PLL chip would be designed for such a purpose. Today's technologies (BiCMOS) have proven to provide the required performance but no IC's are currently available on the market. The concept was proven effective in a lower frequency range where IC's are available. On own funding the project will be continued once IC's for 6GHz and beyond are available.

3.3 Conclusion

Wideband synthesizers with 1 Hz resolution can be designed and manufactured for frequency ranges where PLL IC's are commercially available or funding is provided for custom designs. The synthesizer above would be able to provide the desired frequency range and phase noise with a custom PLL IC. A new method of generating very high purity reference frequencies was successfully implemented which is the core of such a design.

4. High Dynamic Range, Tunable Filters

The goal of this project was to design an ultra-high dynamic range, voltage tuner, and pre-selector filter. The filter requirements are a high third order intercept point (IP3) of at least +40 dBm, use a minimal amount of prime power (<1 mW), and be low cost (several dollars in discrete parts). The desired frequency range is 30 MHz to 3,000 MHz, in several bands.

The key technical difficulty is to obtain the high IP3 value in-conjunction with the low prime power requirement. Current filters use varactor diodes to vary the resonant frequency of the filter circuit. Unfortunately, large RF signals tend to modulate the varactor bias voltage, which causes distortion.

To satisfy the IP3 requirement, we developed three novel circuit techniques. These were investigated extensively using the Ansoft Serenade simulation tool, which accurately models the diode non-linear characteristics. Several of these techniques were then verified using prototype circuits in the 200-400 MHz frequency range.

IP3 values of +40 dBm for each technique were obtained. We believe that combining the techniques (not yet investigated) would provide IP3 values significantly above +40 dBm.

4.1 Baseline Filter Design

A Baseline filter was used to provide a reference for the circuit designs developed in this project. The Baseline filter is shown in Figure 13. This filter uses two resonant "tank" circuits (four varactor diodes in each tank circuit (D1-D4 and D5-D8) along with inductors (L2 and L3)), and three inductors (L6, L7 and L8) to couple the tank circuits together. The varactors are tuned with DC bias lines that use large resistors (R1 and R2) to decouple the tuning and the RF circuits. This filter tunes from 200 MHz to 400 MHz. The pass bandwidth is approximately 10% of the center frequency.

To obtain the 30 MHz to 3,000 MHz tuning range, multiple octave filters would be used. High IP3 RF switches would be used to select the desired filter. This filter design is very compact and is extensible over the desired frequency range. The Baseline filter's shortfall is an IP3 of approximately+24 dBm. The prime power required is very small (mA to bias the varactors).

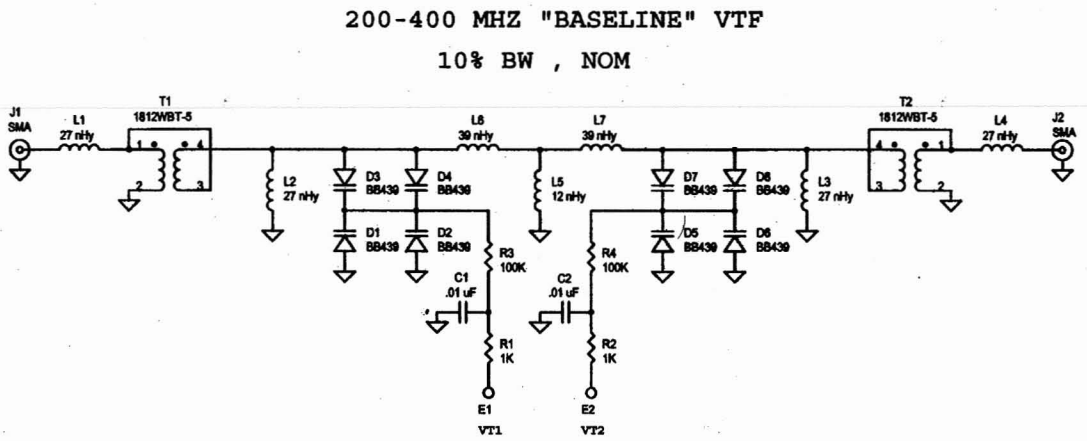


Figure 13: Baseline Tunable Filter Uses Two Varactor Tanks and Inductive Coupling

4.2 Techniques Used to Increase Filter Performance

To increase the Baseline filter's IP3, three circuit techniques were developed. Each of these techniques is discussed in the following sections.

4.2.1 Technique 1 - Many Diodes in Parallel and Series

The first technique to improve the Baseline filter's IP3 is to increase the number of tank varactor diodes in parallel and series. This maintains the capacitance of the varactor tank elements, but reduces the RF voltage in each diode, hence, reduces the distortion. Each (series) doubling of varactors reduces the RF voltage by two. The power handling is improved by 3 dB, and the IP3 is improved by $2^3/2 = 6$ dB.

To verify this, extensive simulations were made and multiple prototype filters was built. A photograph of a prototype circuit board with multiple filter designs in shown in Figure 14. The filter designs labeled "Baseline" and "Alt No 3" are the same except that the number of varactor diodes is doubled in Alt No 3 compared to the Baseline.

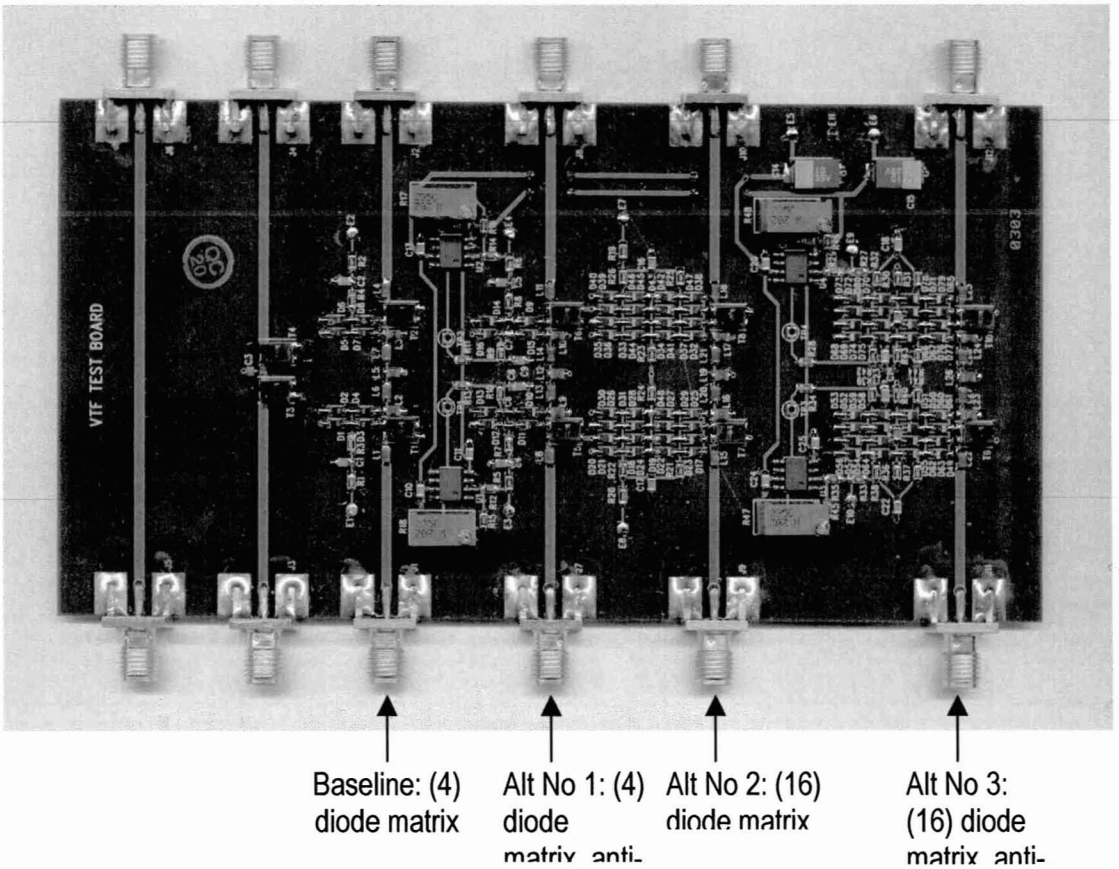


Figure 14: Photograph of Prototype Filter With the Baseline Filter and Versions With Multiple Diodes in Parallel and Series

The measured and simulated IP3 of three different filters with four diodes per tank (Baseline), eight diodes per tank (Alt 3), and 16 diodes per tank (Alt 4) are shown in Table 1. The IP3 values approximately follow the 6 dB rule mentioned previously. The Alt 3 filter's IP3 was 6 dB larger that the Baseline filter's IP3 value. The measured Alt 3 filter's IP3 was 9 dB (ideally 6 dB) larger that the Baseline filter's IP3 value. The Alt 4 filter's IP3 value was 13 dB (ideally 12 dB) larger than the Baseline filter's IP3 value.

Table 1: Measured and Simulated Filter IP3 Values for Different Configurations

BB439	Description	Measured					Simulated					Meas/Sim
300 MHz		S11	S21	IIP3	Delta IIP3	Tune	S11	S21	IIP3	Delta IIP3	Tune	IIP3
		dB	dB	dBm	dB	Volts	dB	dB	dBm	dB	Volts	dB
Baseline	4 diodes/matrix	-18	-3	20		9.5	-21	-4	24		9	4.0
Alt 3	16 diodes/matrix with anti-parallel	-18	-3	29	9	11	-21	-4	30	6	9	1.0
Alt 4	64 diodes/matrix						-19	-5	37	13	9	

A potential difficulty with adding diodes in parallel and series is that the parasitic inductance and capacitance due to circuit board traces limits the filter's tuning range. As diodes are added, capacitance to ground is increased, thus limiting the tuning range and the highest

tuning frequency. At frequencies below 1 GHz, this is not too much of a problem, but above 1 GHz the parasitic values become more significant. We simulated the filter parasitics using the model shown in Figure 15, and then estimated the reduction in filter tuning range caused by the parasitic elements.

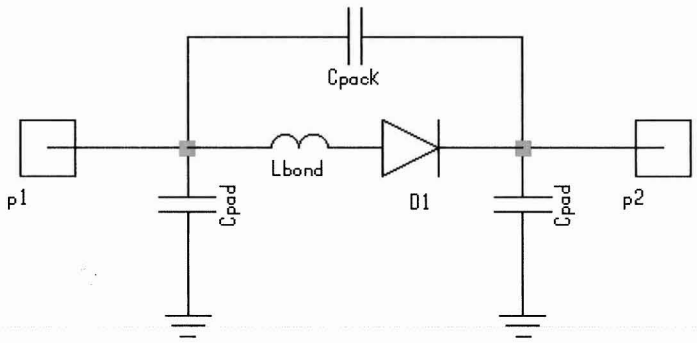


Figure 15: Circuit Diagram Showing Varactor Diode (D1) and Parasitic Circuit Elements

Figure 16, below, shows the filter response of the baseline filter design with and without parasitics. The maximum filter frequency is 405 MHz with parasitics and 460 MHz without parasitics. This is a significant reduction in performance.

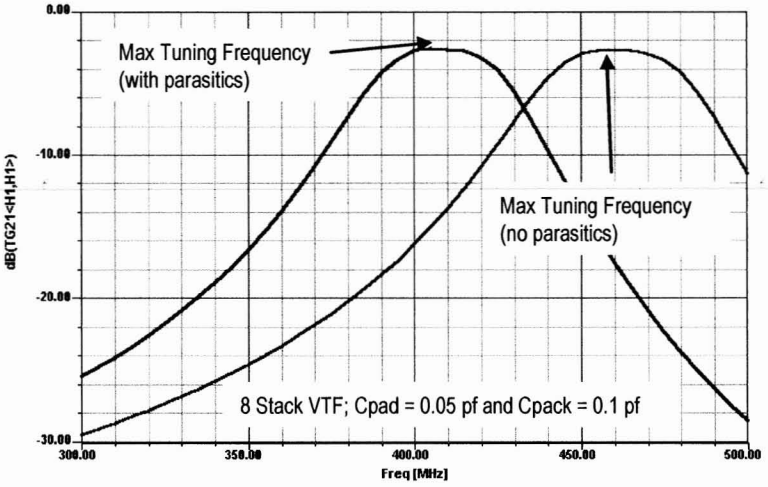


Figure 16: Filter Response at the Maximum Tuning Frequency With and Without Varactor Parasitic Circuit Elements

To investigate the impact at higher frequencies, the Baseline filter design was scaled to operate from 1200 MHz to 2700 MHz. Figure 17 shows the reduction in the maximum tuning frequency due to parasitics of this design is more significant.

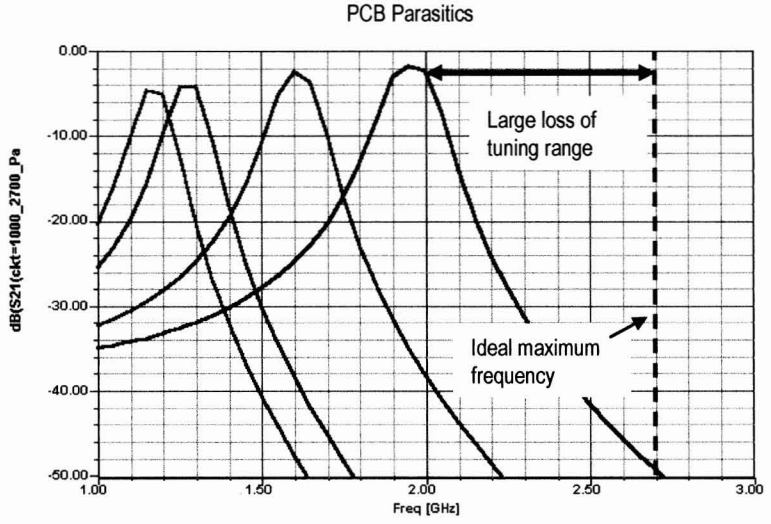


Figure 17: Multi-Varactor Filter (With Discrete Components and a Printed Circuit Board (PCB) Response Versus Frequency (at Different Tuning Voltages) Incurs a Large Loss in Tuning Range Because of the PCB Parasitics

To operate at these higher frequencies with a large number of varactor diodes, an integrated design is required because this greatly reduces the parasitic values. A thin film, Low Temperature Co-fired Ceramic (LTCC) technology technique can be used. We simulated this approach and the filter response versus tuning frequency values are shown in Figure 18. This design only has a small tuning range loss due to parastics. Thus, we believe that it is possible to use the multi-varactor diode approach to improve the IP3 performance, even up to 3,000 MHz.

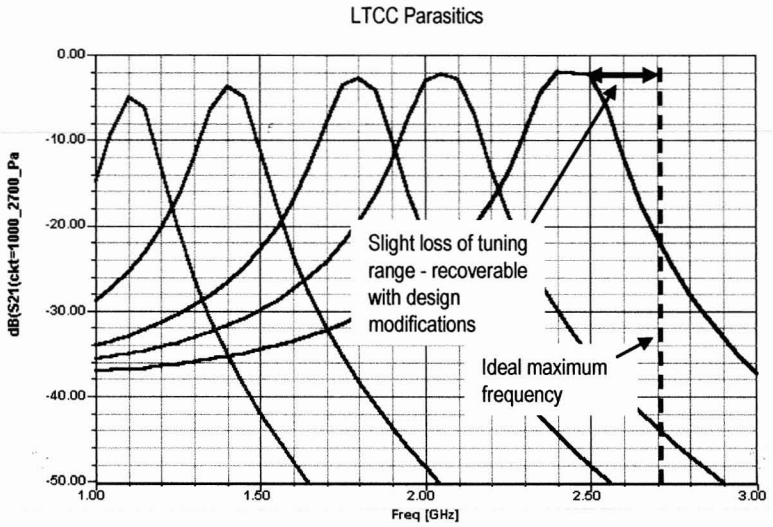


Figure 18: Multi-Varactor Filter (with Integrated Varactors Using Low Temperature Co-Fired Ceramic (LTCC) Technology) Response Versus Frequency (at Different Tuning Voltages) Incurs a Small Loss in Tuning Range Because of the Varactor Parasitics

4.2.2 Technique 2 - Optimum Diode Power Value

The second technique is to align the diodes in a "back-to-back" arrangement, and then to select the diode power-law exponent value to maximize the IP3 performance. As shown in Figure 19, arranging the diodes in the "back-to-back" configuration partially cancels distortion.

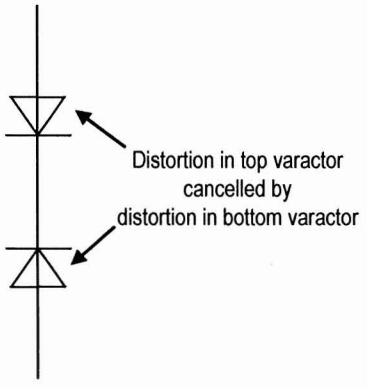


Figure 19: Two Diodes "back-to-back" Create Distortion That Partially Cancels the Distortion

The following equations show the varactor diode capacitance as a function of the tuning voltage. The power-law parameter (m) controls the varactor tuning slope.

capacitance expression used for a PN junction is:

$$C(v) = \frac{C_0}{\left(1 + v/V_b\right)^m} = \frac{K}{(V_b + v)^m}$$

where

$C(v) = dq/dv$	incremental diode capacitance
C_0	zero-bias capacitance
V_b	built-in potential
K	$C_0(V_b)^m$
m	power-law exponent (grading coefficient)
v	voltage from anode to cathode

We conducted extensive simulations using the Baseline filter design and varied the power-law value from 0.3 to 0.8. For each configuration, we determine the filter's IP3 value as shown in Figure 20. The IP3 value is a strong function of the m-value, and the best IP3 occurs with an IP3 value of 0.5.

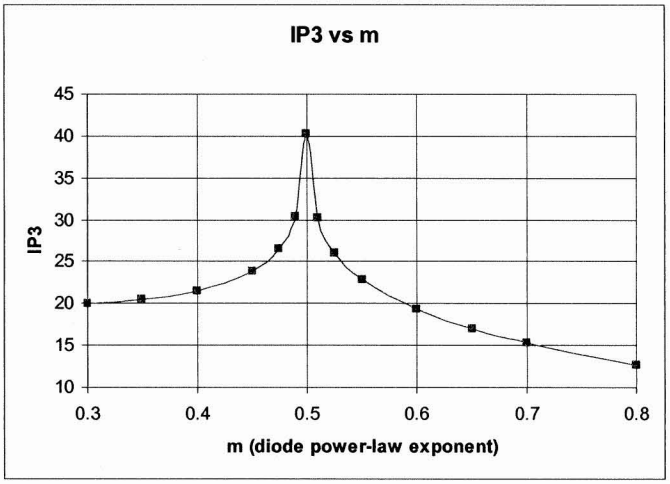


Figure 20: The Baseline Filter Input Third Order Intercept Point (IP3) versus Diode "m" Value Shows That if m=0.5, the Filter IP3 is Maximized

We believe that the two techniques (Technique 1: Many Diodes in Parallel and Series and Technique 2: Optimum Diode Power Value) can be combined to obtain IP3 values of +40 dBm to +50 dBm because the two mechanisms are independent.

4.2.3 Technique 3 - Distortion Cancellation

The third technique is to add a small diode to one side of the varactor tank circuit. This small diode generates distortion currents that cancel the varactor tank circuit distortion. Because the IM current that is not cancelled by the common cathode pairs is very small, the additional diode must provide a very small cancellation current in the correct phase.

The circuit diagram for this approach is shown in Figure 21. The small diode (D2IM) value depends on the tank varactor diode m-value and is found iteratively. For the diode used in this work, the size needs to be about 1/128 that of the tuning diodes.

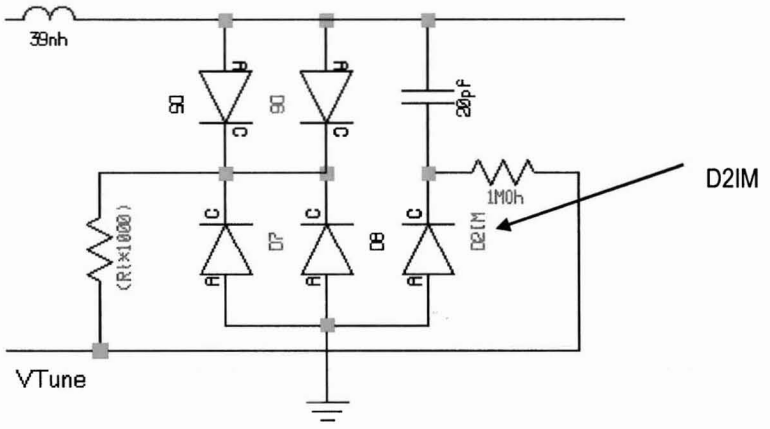


Figure 21: To Increase the IP3 of a Varactor Filter Bank, an Extra Diode (D2IM) is Added to Partially Cancel the Distortion Produced by the Varactors

The position of the small diode in the circuit depends on the varactor diode m-value. The configuration shown is valid for m > ½. For m < ½, the capacitor and diode should be swapped, with the cathode still connected to the bias resistor

Simulations show that an IP3 of 37 dBm to 40 dBm is attainable with this design.

4.3 Conclusions

This project has shown that it is feasible to build a voltage-tuned filter with an IP3 value of +40 dBm using readily available varactor diodes. Three circuit technologies were developed: (1) Adding many diodes in parallel and series, (2) to arrange the diodes "back-to-back" and to select the diode m value to 0.5, and (3) to add an extra diode to cancel the distortion. To increase the frequency range to 3,000 MHz, the diodes need to be integrated so that the parasitic impedances from the circuit connections are reduced. These above techniques have been proven using a combination of simulations and prototype tests.

5 Summary

This final report describes three research and development projects conducted by Synergy Microwave Corporation for DARPA (Defense Advanced Research Agency). The purpose of these projects was to develop and demonstrate the key sub-systems needed for an ultra-high performance, low cost, multi-band tactical transceivers. These devices include: 1) A 25 MHz to 2,500 MHz, 5 W power amplifier, 2) A 2.5 GHz to 6 GHz synthesizer to be used the receiver's first local oscillator, and 3) A 25 MHz to 3,000 MHz tunable filter that can be used as a pre-selector or a post power amplifier filter.

Prototypes of each device were constructed that demonstrated the feasibility of each design concept.

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